for copper (CU) displayed adjacent to the copper interconnection lines **72**. Accordingly, the drawings disclose a metal interconnection line made of copper, and withdrawal of the objection is respectfully requested.

The Office Action rejects claims 1-2, 4-7 and 9-10 under 35 U.S.C. §112, second paragraph, stating that "the role of said shunting interconnection line is unclear". By this amendment, claim 1 is amended to obviate the rejection. Accordingly, withdrawal of the rejection is respectfully requested.

The Office Action further rejects claims 1-2, 4-7 and 9-10 under 35 U.S.C. §112, second paragraph, stating that "it is unclear if said sub lines are the actual word lines of the matrix". This rejection is respectfully traversed.

In particular, Applicant points to the specification, which outlines the functionality and relationship of a main word line and sub-word line with respect to a memory matrix in great detail. See, e.g., Figs. 4A and 4B and page 19, line 2 to page 21, line 21. Further, Applicant asserts that the interrelationship of all the claim elements, including main word lines and sub-word lines, are adequately recited in the claim language to provide an adequate description of the claimed invention under 35 U.S.C. §112, second paragraph. For example, claim 1 recites a plurality of memory cells and respective sub word lines with each sub word line having a corresponding shunting interconnection line, a plurality of main word lines for transmitting a row select signal, and a plurality of sub word drivers that drive corresponding sub word lines and shunting interconnection lines into a selected state according the row select signals. Accordingly, withdrawal of the rejection is respectfully requested.

Office Action rejects claims 1-2, 4-7 and 9-10 under 35 U.S.C. §102(e) over Kawasaki (U.S. Patent No. 6,240,006); rejects claims 1-2, 4-7 and 9-10 under 35 U.S.C. §102(b) over Kawasaki (JP Patent No. 11-354745); and rejects claim 11 under 35 U.S.C. §103(a) over

Kawasaki (JP Patent No. 11-354745) in view of Kometani et al. (U.S. Patent No. 5,748,549). These rejections are respectfully traversed.

In particular, Applicant asserts that none of the applied references, individually or in combination, teach or suggest a semiconductor memory device that includes a plurality of memory cells arranged in rows and columns, a plurality of sub word lines, a plurality of main word lines... disposed in a **first conductive layer** for transmitting a row select signal and a plurality of shunting interconnection lines, provided corresponding to the respective sub word lines in a **second conductive layer** formed **under** said first conductive layer, each shunting interconnection line for electrically connecting to a corresponding sub word line at a prescribed interval and allowing signal transmission between said corresponding sub word line, as recited in independent claim 1.

Japanese Patent Kawasaki (JP Patent No. 11-354745) and U.S. Patent Kawasaki (U.S. Patent No. 6,240,006), which derives its priority and substance from Japanese Patent Kawasaki Kawasaki, will be discussed in tandem, with respective citations from Japanese Patent Kawasaki cited in [brackets].

Kawasaki discloses a semieonductor memory device **1** having a number of main word lines **MWL** with corresponding sub-word lines **SWL**. See, col. 8, lines 40-49 [paragraphs 0057-0058]. However, Kawasaki does not disclose a plurality of main word lines disposed in a **first conductive layer**, for transmitting a row select signal and a plurality of shunting interconnection lines provided in a **second conductive layer** formed **under** the first (main word line) conductive layer, as recited in independent claim 1.

To the contrary, Kawasaki does not disclose any equivalent "second conductive layer" that contains any shunting interconnection lines that couples a main word line and a sub-word line. In fact, the closest, but not equivalent, structure to a shunting interconnection line in

Kawasaki is shown in Fig. 15, i.e., a low-resistance conductive material **76**. As shown in Fig. 15, a word line is formed in a gate electrode layer **72** (see, col. 19, line 38 [paragraphs 0111]) with a low-resistance conductive material **76** (see, col. 19, lines 49-50 [paragraphs 0111]) formed **above** the gate electrode layer **72** (and not under the gate electrode layer **72**) to couple the gate electrode layer **72** and a conductive layer **74** at a region referred to as a word line shunt region.

While the Office Action states that Kawasaki discloses "a plurality of shunting interconnection lines, (Figure 7 #43 & Col. 12 Lines 56-58), provided corresponding to the respective sub word lines in a second conductive layer formed under said first conductive layer", Applicant respectfully asserts that this statement is in error. A review of Fig. 7 and respective text discloses that the cited "shunting interconnection line" is actually a conductive interconnection line **43**, which serves as a bit line, and has no immediate relationship or electrical coupling to conductive interconnection line **10,** which serves as a main word line. See, col. 12, lines 56-58 [paragraph 0078]. This assertion is confirmed by the absence of any sub word drivers connected to conductive interconnection line **43** either in Fig. 7 or any other drawing in Kawasaki.

In comparison with Kawasaki, the present intention locates its main word lines **3A1** above its shunt interconnection lines **1A1**. By using the first level metal interconnection line **7** as a shunting interconnection line, a word line shunting structure can be implemented that enables sub-word lines to be driven at high-speeds, and without adding a manufacturing step, thus simplifying processing. See, page 17, line 17 to page 18, line 1. Accordingly, U.S. Patent Kawasaki does not disclose each and every limitation of independent claim 1.

As Japanese Patent Kawasaki discloses substantially the same structures as U.S. Patent Kawasaki, Japanese Patent Kawasaki similarly does not disclose each and every limitation of independent claim 1.

Komentani discloses a semiconductor memory device having a copper interconnection layer. See, col. 4, lines 10-12. Komentani does not disclose a plurality of main word lines... disposed in a **first conductive layer**, for transmitting a row select signal and a plurality of shunting interconnection lines, provided corresponding to the respective sub word lines in a **second conductive layer** formed **under** said first conductive layer, as recited in independent claim 1, nor does the Office Action assert such. Accordingly, Komentani does not provide for the deficiencies of U.S. Patent Kawasaki and Japanese Patent Kawasaki.

Thus, independent claim 1 defines patentable subject matter. The dependent claims define patentable subject matter by virtue of their dependency as well as for the additional features they recite. Accordingly, withdrawal of the rejections under 35 U.S.C. §102 and 35 U.S.C. §103 is respectfully requested.

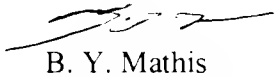
For the reasons given above, Applicant believes that this application is in condition for allowance and Applicant requests that the Examiner give the application favorable consideration and permit it to issue as a patent. However, if the Examiner believes that the application can be put in even better condition for allowance, the Examiner is invited to contact Applicant's representative listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including

extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT, WILL & EMERY



B. Y. Mathis
Registration No. 44,907

600 13th Street, N.W.
Washington, DC 20005-3096
(202)756-8000 BYM/SAB:kap
Facsimile: (202)756-8087
Date: January 24, 2003

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claim 1 has been amended as follows:

1. (Amended) A semiconductor memory device comprising:

a plurality of memory cells arranged in rows and columns;

a plurality of sub word lines, provided corresponding to the respective memory cell rows, each having memory cells on a corresponding row connected thereto;

a plurality of main word lines, each provided corresponding to a prescribed number of sub word lines in said plurality of sub word lines and disposed in a first conductive layer, for transmitting a row select signal;

a plurality of shunting interconnection lines, provided corresponding to the respective sub word lines in a second conductive layer formed under said first conductive layer, each shunting interconnection line for electrically connecting to a corresponding sub word line at a prescribed interval and allowing signal transmission between said each and said corresponding sub word line; and

a plurality of sub word drivers, provided corresponding to the sub word lines, each for driving a corresponding sub word line and a corresponding shunting interconnection line into a selected state according to at least a row select signal on a corresponding main word line.

Please add new claim 12 as follows:

-- 12. (New) The semiconductor memory device according to claim 1, wherein said plurality of shunting interconnecting lines are each electrically connected to the corresponding sub word line through contacts formed at said prescribed interval.--